INTRODUCTION TO LOW POWER RF-IC DESIGN

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PART – I
Basics of RF Design

WHAT IS RF?
Frequency spectrum:

- Why Lumped parameters models failed
- Kirchoff's to Maxwell's
- Failure of two port circuit parameter (Z, Y, ABCD)
- Scattering parameter (S-parameter) on the basis of Maxwell equation comes in...

Application area of the RF-IC designer

- Wireless communication
- Radar
- Navigation
- Remote sensing
- RF identification
- Automobile and Highways
- Sensors:
  - Medical
  - Radio-astronomy and space exploration

Beauty of RF IC Design:
Link between Microwave Engineer and Design Engineer

Maxwell equation's are
\[ \mathbf{\nabla} \times \mathbf{E} = -\mu \mathbf{H} \mathbf{t} \]
\[ \mathbf{\nabla} \cdot \mathbf{H} = \epsilon \mathbf{D} \mathbf{t} \]
\[ \mathbf{\nabla} \cdot \mathbf{E} = 0 \]
\[ \mathbf{\nabla} \times \mathbf{H} = \mu \mathbf{E} \mathbf{t} \]
Kirchoff's law
- Total voltage around a loop is zero (KVL)
- No net current build up at any node (KCL)

Comparison of Analog and RF/MW

1. On Discrete PCB component

(a) Analog [Low frequency<100MHz]
- Conductor
- Capacitor
- Resistor
- Inductor

(b) RF/MW [High frequency>100MHz]
- Microstrip line
- Ceramic
- Thin Film
- Thin Film SMD comp.

*As the physical dimension of circuit element & sub-circuit in a IC chip is very less (even less than 1/10th of λ, 30 cm in air at 1 GHz), so transmission of wave of light is not noticeable inside chip, so a full transmission line (Microwave) for on-chip design and analysis is generally unnecessary. Kirchoff's law is well suited for on-chip design.

*But for interfacing the RF signals in / out of the chip, we need connectors, boards, cables etc. Where transmission-line effects cannot be ignored.
Comparison of Analog and RF/MW

1. **On Performance Based**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Analog (Low frequency&lt;100MHz)</th>
<th>RF/MW (High frequency&gt;100MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A. Small signal AC equivalent circuit analysis</td>
<td>A. Small signal AC equivalent circuit analysis with parasitic, i.e. Good circuit Modeling</td>
<td></td>
</tr>
<tr>
<td>B. Linearity</td>
<td>B. Matching</td>
<td></td>
</tr>
<tr>
<td>C. Stability</td>
<td>C. Noise</td>
<td></td>
</tr>
<tr>
<td>D. Noise (in few cases)</td>
<td>D. Stability</td>
<td></td>
</tr>
</tbody>
</table>

A. **Small signal AC equivalent circuit analysis with parasitic**

- Good circuit Modeling

B. **Matching**

- E. Linearity
- F. Sensitivity
- G. Dynamic range

Comparison of MMIC/RFIC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MMIC (Discrete)</th>
<th>RFIC (integrated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Development Cost</td>
<td>Moderate</td>
<td>Very high</td>
</tr>
<tr>
<td>Modifications</td>
<td>Relatively easy &amp; inexpensive</td>
<td>Expensive, generally one or more new mask</td>
</tr>
<tr>
<td>BOM cost</td>
<td>Low</td>
<td>Depends on volume, die size and process used</td>
</tr>
<tr>
<td>Mixing Technologies</td>
<td>Optimum device technology can be used through out (combined GaAs, RF, MMIC)</td>
<td>Limited scope</td>
</tr>
<tr>
<td>Parts Count</td>
<td>High</td>
<td>Low to very low</td>
</tr>
<tr>
<td>Size</td>
<td>Small to medium</td>
<td>Smallest</td>
</tr>
<tr>
<td>Weight</td>
<td>Light</td>
<td>Lightest</td>
</tr>
<tr>
<td>Cost of Using Additional transistor</td>
<td>Moderate</td>
<td>Low</td>
</tr>
<tr>
<td>Matched transistor</td>
<td>Difficult to implement</td>
<td>Very good, used extensively</td>
</tr>
</tbody>
</table>

Basic of RFIC design

- Disciplines required in RF design

- Analog/RF design octagon

- Disciplines required in RF design

RF CIRCUITS AND SYSTEMS - DESIGN ISSUES

1. Phase shift of the signal is significant over the extent of the component because it’s size is comparable with the wavelength.

2. The reactance of the circuit must be accounted for, particularly those associated with the parasitic of the active devices.

3. Circuit losses causes degradation of Q, reduction of frequency selectivity and noise performance.

4. Noise especially arising from the circuit can be significant and it’s effect needs to be modeled.

5. Electromagnetic radiation, capacitive coupling and substrate coupling significantly alter the performance of the circuit.

6. Reflection issues, because circuit size is of the order of a wavelength.

7. Circuit design should take care to ensure reflections do not cause any loss of gain, power, or failure of components.

8. Nonlinearities which cause distortion and unwanted frequency components is undesirable, but it may become essential part of the circuit operation, as in mixing or local oscillators.

Noise

**Significance**: The significance of noise performance of a circuit is the limitation it places on the smallest input signals the circuit can handle before the noise degrades the quality of output signal.

- **Thermal Noise**
  - Brownian motion of thermally agitated charge carriers is generated in every physical resistor
  - 
  - Pure reactive components generate no thermal noise

- **Shot Noise**
  - Gaussian white process associated with the transfer of charge across an energy barrier
  - Due to DC current through p-n junction, gate channel

- **Flicker noise in MOSFET**
  - Random trapping of charge at oxide interface
  - Modeled as a voltage source in series with gate

Gate induced noise

Thermal agitation of channel charge cause fluctuation of channel potential. This causes a negligible with gate terminal, leading to gate noise

- + δ – 4/3 in long device
- Both drain and gate noise share a common origin and they are correlated

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- Gaussian white process associated with the transfer of charge across an energy barrier
Noise figure

Noise figure (F) specifies the noise performance of a circuit or device.

- **Limitation**: Noise figure is definable only when input source is resistive — important parameter on communication system as the source impedance in this system is often resistive.

- **Definition**:

  \[ \text{Noise factor (NF)} = 10 \log_{10} \text{NF} \]

  - Noise figure measures the SNR degradation as a signal passes through a system.
  - If a system has no noise, NF = 1, F = 0 dB.
  - If input signal contains no noise then SNR = 0 dB.
  - NF = \( \alpha \) (even though the system has finite noise), is it really possible?

- **Examples**:

  - Noise factor = Loss
  - Noise factor = Noise figure of cascaded stages

  Noise figure of cascaded stages:

  \[ \text{NF}_{\text{total}} = \text{NF}_1 + \text{NF}_2 + \cdots + \text{NF}_n \]

  For m stages:

  \[ \text{NF} = \text{NF}_1 + \text{NF}_2 + \cdots + \text{NF}_n \]

- **Noise figure of Lossy circuit**:

  \[ \text{Noise figure} = \frac{\text{Input noise power}}{\text{Output noise power}} \]

- **LINEARITY ISSUES**

  - Linear system: output can be expressed as a linear combination of input.
  - Non-linear system: output cannot be expressed as a linear combination of input.
  - Time invariant system: Time shifts do not change the input-output relationship.
  - Time varying system: Time shifts change the input-output relationship.
  - Differential or balance system: system with a single input.

Examples:

- Output noise current due to source resistance:

  \[ I_{\text{noise}} = g_m V_{\text{noise}} \Delta f \]

- Total output noise current:

  \[ I_{\text{noise}} = g_m A F_\Delta f + I R_g + I R_f + I R_c \]

- NF calculation:

  \[ \text{NF} = 1 + \frac{g_m A F_\Delta f}{g_m A F_\Delta f + g_m A R_g + g_m A R_f + g_m A R_c} \]

- Noise figure of cascaded stages:

  \[ \text{NF}_{\text{total}} = \text{NF}_1 + \text{NF}_2 + \cdots + \text{NF}_n \]
Linearity Issues Cont...

- Nonlinearity, nonlinearity system
  - For a nonlinear system that can be approximated by
    \[ y(t) = ax(t)^n \]

- Harmonics
  - \( f \) is the input frequency, then
    \[ f_2 = 2f, f_3 = 3f, \ldots \]

- Gain Compression
  - Fixed signal pairs vary with input level
  - Fixed circuits do compression or overloading
    \( V_{in} > V_{out} \)

- Distortion signal gain decreases function of \( f \)
  - A nonlinear compression input signal level that
    causes small signal pairs to drop by 1 dB

- Non-adjacent harmonics: second harmonic, even order
  - An odd harmonic consists of even harmonics, square root, and other terms proportional to
    higher power at \( f \)

- Nonlinear gain for small \( f \) harmonic is given in proportion to \( f^2 \)

20log \( I_{IP3} \) dB = 30dB

\[ I_{IP3} = 10 \text{dB compression point} \]

Method for Estimating Linearity Parameter from Device Parameter

Already we get for a nonlinear system

\[ I_{IP3} = \frac{V_{in}}{V_{out}} \quad \text{and} \quad \text{MOSFET current} \]

\[ I_{IP3} = \frac{g(V_0)}{g(V_+) \quad g(V_-)} \]

- Transconductance value, where \( V_0 \) is the dc-bias voltage, \( V_+ \) is slightly higher and \( V_- \) is slightly lower

Stability Analysis

Basic criteria: For good stable has no positive feedback loop, in general

- CS-stage
  \[ V_{out}(s) = \frac{V_{in}(s)}{1 + \frac{1}{sC_{gs}}} \]
  - \( C_{gs} \) gives pole in right half plane, \( sC_{gs} \to 0 \), then get good stability

- CG-stage
  \[ V_{out}(s) = \frac{V_{in}(s)}{1 + \frac{1}{sC_{gd}}} \]
  - \( C_{gd} \) gives pole in right half plane, \( sC_{gd} \to 0 \), then get good stability

- The backward transmission (S21) is required to be small for good stability

- As real circuits are complex, proper analysis of transfer function is required and
  compensation techniques is used to obtain good stability (such as OPAMP)

Sensitivity

- Definitions
  - Minimum signal level that a system can select
  - \( P_{in} \) is the input power
  - \( P_{out} \) is the output power
  - \( B_{in} \) is the input bandwidth
  - \( f_{in} \) is the input frequency
  - \( f_{out} \) is the output frequency
  - \( B_{out} \) is the output bandwidth
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- \( f_{in} \) is the input frequency

- \( f_{out} \) is the output frequency

- \( B_{out} \) is the output bandwidth

- \( f_{in} \) is the input frequency
**Dynamic Range**

- **Definition:**
  \[ \begin{align*}
  \text{Gain} &= \frac{\text{Output}}{\text{Input}} \\
  \text{S/N (Signal-to-Noise Ratio)} &= \frac{\text{Power in the signal}}{\text{Power in the noise}} \\
  \text{THD (Total Harmonic Distortion)} &= \frac{\text{Power of harmonics}}{\text{Power of the fundamental}} \\
  \text{Distortion} &= \frac{\text{Power of distortion}}{\text{Power of the sinusoidal signal}}
  \end{align*} \]

- **Equation:**
  \[ \text{Gain} = \frac{V_{out}}{V_{in}} \]

**High Frequency Device modeling**

- **Silicon Technologies:**
  - Bipolar
  - BiCMOS
  - MOS

**WHY CMOS FOR RF-IC**

- **Standard Digital CMOS is hardly the ideal medium for RF ICs, because of:**
  - Lossy Silicon substrate
  - Large source/drain parasitics
  - High device noise and poor 1/f noise performance
  - Series gate resistance

- **But,**
  - Device scaling is faster
  - CMOS fT (and fmax) doubles roughly every 3 years.
  - CMOS is cost effective
  - Both digital & analog block can be designed on same substrate
  - High linearity; Low distortion
  - Low power consumption
  - On-chip realization of passive inductors and capacitors

**Visualize of Process Flow**

- **CMOS vs BJT**
  - Higher gain for same bias.
  - Higher fT.
  - Low thermal and 1/f noise, but input current noise.
  - Linear DC offsets.
  - Lower overdrive (Low VCE sat).
  - Lower DC offset.
  - No body effect.
  - Better scaling properties.

**RF CMOS MODELLING**

- "Standard" (digital oriented) MOS models do not allow for RF.

- To calculate magnetic coupling between two adjacent metal lines, interlayer capacitance, EMI between substrates & on-chip passive component (such as inductor and MOS capacitor), the Maxwell EM equation is required (Challenging issue!!!)

- In RF, Cgs (whose effect negligible in low frequency analog) affects the matching with successive blocks. Frequency dependence of Transconductance(gm)
RF CMOS Modelling

Active Inductor Design

Key Issues:
- Z(s) = \frac{1}{LS} + \frac{1}{R}
- Concerned properties: Bandwidth, Quality Factor (Q) and Noise Factor.
- Advantages over Spiral Inductors:
  - High Q factor (about 5 times)
  - Less parasitic effect
  - Much Less Chip Area
- Disadvantages: Bandwidth is Low, Higher Noise.

Coplanar Spiral Inductors

Most Popular structure → Coplanar Spiral Inductor
- Shapes Used → Rectangular, Circular, Polygon
- Disadvantages:
  - Low Q → Metallic ohmic loss, Substrate losses, Eddy current loss
  - Poor Quality factor (Typically 3-6)
  - Takes large area
  - Noisy → Thermal noise of various resistors (Metal, Eddy current, Substrate)

Coplanar Spiral Inductor Design

Design Parameters:
- Edge to Edge distance \( d \) (Typically 100-200 \( \mu m \))
- Metal strip width \( w \) (Typically 10-15 \( \mu m \))
- No of turns (Typically 3-5)
- Strip Separation \( t \) (Typically 1-3 \( \mu m \))

Technology Constraints:
- No of Metal Layers (Typically 3-5)
- Metal Layer Thickness (or Metal Sheet Resistance)
- Substrate Resistivity

Design Guide-Lines:
- Hollow structure gives better Q
- Top metal layer used (Small substrate Cap, Low Metal Resistivity)
- Pattern Ground Shield (Reduces Eddy Current Loss)
- Self Resonance Frequency \( \omega_0 = \frac{1}{\sqrt{LC}} \) is \( \omega > \omega_0 \) Operating Frequency

On-Chip Passive Component

On-Chip Inductor Realization

- At RF frequencies, matching network consists of number of inductors. Therefore on-chip realization of inductors is important for RF IC design.
- Three kind of inductors:
  - ACTIVE INDUCTOR → More noisy, highly non-linear, High Q with large L value possible, frequency dependent, higher power consumption.
  - BOND WIRE INDUCTOR → Depends on curvature, High Q (~60), Typical value: 1nH/mm, series resistance: 0.2\( \Omega \) mm (1mm)².
  - ON-CHIP SPIRAL INDUCITOR → Less Q (~3-6). In CMOS process maximum 10nH value possible with reasonable Q values, very small DC power consumption. At very low (<0.5nH) L value → interconnect parasitics dominate… At high (>10nH) L values → Large area, High losses.
**Typical Bond Pad capacitance is of the order of 300 – 600 fF.**

**Shielding reduces the effect of loss (due to Rsub).**

**PART – II**

**Transceiver Design**

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**Basic Transceiver Architecture**

- **T/R Switch**
- **LNA**
- **Down Converter**
- **Up Converter**
- **Frequency Synthesizer**
- **PA**

**Performance Measures**

**Transmitter**
- Power efficiency
- Modulation accuracy
- Carrier leakage
- Power consumption

**Receiver**
- Sensitivity
- Selectivity
- Noise
- Dynamic Range
- Linearity
- Power consumption

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**Standards**

<table>
<thead>
<tr>
<th>Standards</th>
<th>GSM</th>
<th>Bluetooth</th>
<th>Zigbee</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Transmission scheme</strong></td>
<td>TDMA &amp; FDD</td>
<td>FHSS/FSK (Frequency Hopping Spread Spectrum)</td>
<td>DSSS/DS-CK (Direct Sequence Spread Spectrum)</td>
</tr>
<tr>
<td><strong>Frequency Band</strong></td>
<td>890 - 915 MHz</td>
<td>2.4 GHz</td>
<td>2.4 GHz, 915 MHz, 868 MHz</td>
</tr>
<tr>
<td><strong>Modulation scheme</strong></td>
<td>GMSK (Gaussian Minimum Shift Keying)</td>
<td>QPSK (Quadrature Phase Shift Keying)</td>
<td>QPSK (Quadrature Phase Shift Keying) or BPSK (Binary Phase Shift Keying) depending on the freq band</td>
</tr>
<tr>
<td><strong>Sensitivity</strong></td>
<td>-90 dBm</td>
<td>-70 dBm (for 0.1% BER)</td>
<td>-85 dBm (2.4GHz) or -92 dBm (915/868 MHz) for packet error rate &lt; 0.1%</td>
</tr>
<tr>
<td><strong>Transmitted power</strong></td>
<td>0.5 – 20 W</td>
<td>Minimum 100 mW, 2.5 mW or 1 mW depending on class</td>
<td>Maximum capability: 0.5 mW, Maximum as allowed by local regulations</td>
</tr>
<tr>
<td><strong>Data Rate</strong></td>
<td>270 KBPS</td>
<td>1 MBPS</td>
<td>250 KBPS, 40 KBPS or 20 KBPS (depending on frequency band)</td>
</tr>
</tbody>
</table>

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**Transmitter Architecture**

- Modulation and upconversion are done in the same circuit
- Simplicity lends it to high degree of integration

**Important drawback:** Output of the PA tends to shift the LO output as its spectrum lies around LO frequency.

- LO Pulling by PA
Transmitter Architecture (contd.)

- Direct Conversion Tx with offset LO
  - LO pulling is avoided by having the PA output spectrum sufficiently away from that of LO

- Two step Transmitter
  - Quadrature modulation of I and Q signals are done at a lower frequency and thereafter the upconversion occurs at higher frequency.
  - PA spectrum is away from both the LO frequencies

Wide-band Transmitter Architecture

- Ultra Wide-band (UWB) Transmitter

Receive Architecture on Application Basis

- Single Band
- Multi-Band
  - Another option for multi-band implementation is to use LNA tuned at two different frequencies

Architecture classification based on principle of downconversion

- Heterodyne Architecture
  - Heterodyne architecture has been the dominant choice for many years.
  - The received signal is first downconverted to an Intermediate Frequency (IF).
  - Received signal is bandpass filtered and downconverted at progressively lower frequencies to achieve high selectivity.
  - Stringent requirements on the filters force the use of large passive components and make it difficult to integrate on a chip.

Problem of Image

- Images can be several times larger than the wanted signal mandating an Image Rejection Ratio (IRR) of at least -70 dB.
- Very high Q requirement is usually placed on the Image Reject Filter

Homodyne Receiver

- Simple Homodyne or Direct Conversion Receiver
  - Simplicity lends it to efficient on-chip implementation
  - Problem of image is not there.
  - To be more precise “images” in this case comes from the same channel and hence are of comparable magnitude as the desired signal. Hence IRR of around -40 dB is typically sufficient.
**Demerits of DCR**

- LO Leakage from LO to RF port and subsequent self mixing produces DC Offset.
- Offset voltages near DC corrupts the signal and more importantly may saturate the following stages.
- LO Leakage also generates spurious radiations.
- Flicker Noise becomes more prominent at low frequencies.
- Even-order distortion

**Image Reject Architectures**

- Special Image Reject architectures were developed to relax the required performance of the filters.
- Image Rejection using Single Sideband Mixing.

**Low IF Architecture**

- Combines the advantages of the heterodyne and homodyne architectures.
- Image rejection is deferred till the IF stage and is done by a filter with asymmetric frequency response.
- Signal and the image are downconverted at positive and negative frequencies respectively or vice versa.
- The image is filtered out by the polyphase filter.

**From system level to component level specifications**

- Initial Guess
- Block Level Spec
- Modify
- System Level Spec
- Requirement Satisfied?
- Final Block Level Spec

**Noise Figure of the Front-end**

- **Given**
  - SNR_{req} Required = 14 dB
  - Sensitivity Required P_{in,min} = -90 dBm
  - Bandwidth = 2 MHz
- The required Noise Figure of the receiver front-end is calculated from the sensitivity eqn.

\[
-90 = -174 + 10 \log_{10}(2 \times 10^{3}) + NF + 14
\]

\[
NF = 7 \text{ dB}
\]
Gain, NF and IIP3 of cascaded stages

- Total Gain:
  \[ A_p = A_{p1} \times A_{p2} \times L \times A_{pk} \]

- Total Noise Factor:
  \[ NF = NF_1 + \frac{NF_2 - 1}{A_{p1}} + \frac{NF_3 - 1}{A_{p1}A_{p2}} + \ldots + \frac{NF_k - 1}{A_{p1}A_{p2} \ldots A_{pk-1}} \]

- Total IIP3:
  \[ IIP_3 = IIP_{31} + IIP_{32} + \ldots + IIP_{3(k-1)} \]

Where \( NF_1, A_p, \) and \( IIP_3, \) are respectively Noise Factor, Available Power Gain and input 3rd order intercept point of the 1st stage.

Example - Gain and NF calculation

ON-CHIP GHZ
CMOS LOW NOISE AMPLIFIER

Characteristics:
- First gain stage in receiver
- Received signal very weak (~μV)
- Gains usually moderate (10-20 dB typical)
- Noise Figure (NF) should be as low as possible (~1 dB)
- Linearity is also an issue
- Reverse Isolation should be high

Design consideration:
- Noise Figure: 2-3 dB
- Gain: 15-20 dB
- IIP3: ~10 dBm
- Input/output Impedance: 50 Ohm
- Input/output Return Loss: ~15 dB
- Reverse Isolation: >30 dB
- Stability Factor >1

LOW NOISE AMPLIFIERS

WHY ON-CHIP?
- 4 P-words:
  - Price: Mass volume production reduces price
  - Package: Integration reduces No of total pin count
  - Performance: Improves except few cases
  - Power: On-chip components dissipate lesser power

Challenges:
- Poor quality of passive components (inductor etc.)
- Device modeling at RF frequencies
- Realizing good analog circuits in digital technology
- Meeting stringent performance requirements in digital environment. Substrate noise coupling is more critical in mixed signal

Different structure of CMOS LNA

Disadvantages of this circuit:
- Due to \( R_{in} \), the power divide by 2.
- NF ~ 1 + (γ/α) * R_{load} / R_{in} > & α (\beta_{m} / \gamma_{m})
- Due to Cgd reverse isolation (S11) Band.
- Due to Cgd effects stability due to presence of zero in transfer function (Vout/Vin).
**Most popular LNA topology**

- **Cascode source degeneration common source**

  ![Diagram](image)

  - Gate of M2 is ac ground, so Gate of M2 is ac ground, so $\frac{1}{g_m}$ effect gets reduced.

  - As impedance looking to source of M2 is $1/g_m$, a resultant Miller capacitor gets reduced.

  - **Choosing of device (W/L) & Vgs**: determine $g_m$ & $C_{gs}$, then $L$ and $L_g$ can be found.

  - **Effect of channel resistance & gate resistance**:
    - modify above equation. (Finding is done in layout to reduce this value).

  - The parasitic of inductor must be considered for calculating practical component values.

  - **Equation for choosing input matching network component**
    - $\frac{1}{g_m} = \frac{1}{g_m} + \frac{1}{g_m}$

  - From Eq. find out equivalent $L_d$ by AUTOC with minimum possible $Q$. Then calculate $C$ from $L_d$, select substrate $C_x$ must larger: $W$ times of $C_x$.

**Bias & Device size**

- **Two-port noise model**

  ![Diagram](image)

  - The channel noise & gate induced noise $I_f$ & $I_f$ are main noise source in MOS.

- **Simplified form**

  ![Table](image)

  - **Power constraint**
    - Noise minimum
    - Without Power constraint
    - Noise minimum

    - The $F_{min}$ differ from $F_{min}$ about 0.5dB to 0.7 dB more($\approx 1$)

    - But the $F_{min}$ are more reliable one from practical circuit design point of view.

    - Without Power constraint

    - $W_{opt}= \frac{1}{(1/C_{gs})}$

    - It is difficult to achieve maximum gain, minimum power consumption, minimum noise figure & good input match at a single value of $W_{opt}$ & bias ($V_{gs}$)......we are now working to develop efficient algorithm for setting global optimum for different constraints.

**Other LNA Structures**

- **Common gate LNA structure**

  ![Diagram](image)

  - This is a common gate topology, the impedance looking from source end is $1/g_m$. This should be made Stohm for matching (active matching).

  - The $L_s$ cancels the $C_{gs}$ value.

  - The noise figure is poor.

  - Good linearity.

- **Complementary LNA structure**

  ![Diagram](image)

  - This is an inverting amplifier topology.

  - Large gain $[-(g_m+1/g_m)]$.

  - Bias current reuslable.

  - Relatively small bias current for identical gain.

  - The noise figure is poor.

**Noise (cont’d)**

- **Differential LNA**

  ![Diagram](image)

  - The single ended LNA (especially for source degeneration topology) is a crucial since degeneration inducer value is small → parasitic dominates in operation.

  - The ground inducer can be tuned by putting extra cap across ground line inducer, but any cap in source line produces a negative resistance in input.

  - **Remedy **→ Differential structure
**INTER-STAGE MATCHING LNA**

- Provides better gain
- Relatively low noise Figure
- Provides 50 Ohm input/output impedance
- Minimum power dissipation

![Schematic](image)

- Provides a negative resistance & extra inductance at IF
- Matching condition changed

**I V Low Noise Amplifier**

- Native MOSes used to facilitate low voltage operation
- The input N/M consisting of $L_p$ and $C_{inp}$ is tuned to 900 MHz.
- The LC load is also tuned to 900 MHz.
- Gate induced noise is included in simulation by an equivalent resistor.

**1 V Low Noise Amplifier Performance Parameters**

<table>
<thead>
<tr>
<th>Performance Parameter</th>
<th>Values in the typical corner</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1 Volt</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>825–975 MHz</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>16.53 dB</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>4.06 mW</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>2.327 dB</td>
</tr>
</tbody>
</table>

**ON-CHIP GHz Oscillators**

- Used for channel selection.
- Frequency depends on Input Control Voltage.
- Frequency change is made by tuning passive elements (e.g. varactors in LC oscillators) or by changing current/voltage supply (e.g. in ring oscillator).
- Governing Equation is:

$$Fout = K_{vco} \cdot V_{control}$$

Here: $K_{vco} = VCO \text{ Gain (Hz/volt)}$, $V_{control} = \text{Input Control Voltage (volts)}$.

**VCO Specifications**

- Center Frequency: $f_0$ (GHz)
- Tuning Range (MHz)
- Tuning Sensitivity; $K_{vco}$ (Hz/volt)
- Spectral Purity or Phase Noise (dBc/Hz @ Hz offset)
- Power Consumption (mW)
- Output Power (mW)
- Harmonic Suppression (dBc)
- Load Pulling : Frequency changes with Load changes
- Supply Pulling : Frequency change with $V_{dd}$ (Hz/volt)

**Types of Oscillators**

- Oscillators are autonomous circuits that produce periodic output without any periodic input.
- Three main topologies and their Comparison:

<table>
<thead>
<tr>
<th>TYPE</th>
<th>Principle</th>
<th>On-chip?</th>
<th>GHz?</th>
<th>PN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ring</td>
<td>Cascaded inverters</td>
<td>YES</td>
<td>YES</td>
<td>POOR</td>
</tr>
<tr>
<td>Relaxation</td>
<td>Cap is charged and</td>
<td>YES</td>
<td>YES</td>
<td>POOR</td>
</tr>
<tr>
<td></td>
<td>discharged</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LC-Tuned</td>
<td>LC resonance</td>
<td>YES</td>
<td>YES</td>
<td>GOOD</td>
</tr>
</tbody>
</table>
QVCO Architecture

VCO Core: LC negative Resistance Oscillator

VCO Core: Salient Features

Frequency Divider

Comparison with other results

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.25 μm</td>
<td>0.18 μm</td>
<td>0.18 μm</td>
<td>0.18 μm</td>
</tr>
<tr>
<td>Supply (Volt)</td>
<td>2.5</td>
<td>1.8</td>
<td>1.5</td>
<td>1</td>
</tr>
<tr>
<td>Tuning Range (GHz)</td>
<td>1.71–1.99</td>
<td>1.05–1.39</td>
<td>0.667–1.156</td>
<td>0.825–0.975</td>
</tr>
<tr>
<td>K_{VCO}(MHz/V)</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>58</td>
</tr>
<tr>
<td>Phase Noise (MHz)</td>
<td>-143@3 MHz</td>
<td>-137@3 MHz</td>
<td>-124@ 600kHz MHz</td>
<td>-136@ 3 MHz</td>
</tr>
<tr>
<td>K_{VDD}(MHz/V)</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>6</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>20</td>
<td>5.4</td>
<td>30</td>
<td>3.5</td>
</tr>
<tr>
<td>FOM (dBc/Hz)</td>
<td>-185.5</td>
<td>-180.96</td>
<td>--</td>
<td>-180.1</td>
</tr>
</tbody>
</table>

Simulation results: Plots

Output waveform of VCO and QVCO

Phase noise

Tuning curves

Variation of frequency and K_{VCO}(MHz/V) with supply voltage
**System simulation results**

![Image of noise figure and IF output for 1 mV RF input]

**Measurement Results (VCO) (contd.)**

<table>
<thead>
<tr>
<th>PMOS Gate Bias (mV)</th>
<th>Output Power (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.362</td>
<td>-23</td>
</tr>
<tr>
<td>0.411</td>
<td>-24</td>
</tr>
<tr>
<td>0.452</td>
<td>-27</td>
</tr>
<tr>
<td>0.519</td>
<td>-36</td>
</tr>
<tr>
<td>0.526</td>
<td>-60</td>
</tr>
</tbody>
</table>

Output Power variation with bias
Output spectrum and phase noise measurement

---

**MIXERS**

- **Ideal Mixer**
  - Multiply signals.
  - Mixer is a Frequency translator circuit.

- **Basic Mixer operation and its MOS equivalent**

\[
\text{Acos}(w_1t) \cdot \text{Bcos}(w_2t) = \frac{AB}{2} \left[ \cos(w_1+w_2)t + \cos(w_1-w_2)t \right]
\]

**MIXER**

- **Classification**
  - On the basis of operating mechanism:
    - **Switching type**
      - Switch the RF signal path ON & OFF at LO frequency.
    - **Non linear type**
      - Use the non linear characteristic of device.
  - On the basis of gain of a mixer:
    - **Passive mixer**
      - Switch type, conversion gain less than one, less noise.
    - **Active Mixer**
      - Nonlinear type, conversion gain greater than one, more noise.

**Special considerations for Mixer Design**

- Provides efficient frequency translation.
- Low noise figure (10-13 dB).
- A moderate conversion gain (8-15 dB).
- Low LO coupling to RF Port (10-20 dB).
- High linearity (-6 – 15 dBm, IIP3).
- Suppression of LO feed-through to the IF port.
- Provides good image rejection (some times require to add image rejection filter).
- IF matching.
- Low distortion.
- Power consumption (3-5 mW) and Area consideration.
Different topologies of CMOS Active Mixer

1. **Square law MOSFET Mixer**
   - RF signal drives the gate while LO drives the source.
   - For long channel devices:
     \[ i_d = \frac{\beta}{2} (V_{gs} - V_T)^2 \]
   - Useful term is the product of \( \cos(w_{RF}t) \) and \( \cos(w_{LO}t) \).
   - All other terms are removed by filtering.
   - The output contains a dc part, RF and LO feed-through, and number of harmonics.
   - Conversion gain:
     \[ \frac{\beta}{2} (V_{LO}) \]
   - For short channel devices:
     \[ i_d = \alpha (V_{gs} - V_T) \]
   - So it can not be used.

**Drawbacks**:
- High chances of LO to IF feed-through, poor port isolation between RF, LO & IF.

Different topologies (continued)...

2. **Single balanced mixer**
   - Output is balanced to RF signal.
   - Exhibits superior performance.
   - Ideally generates inter-modulation terms.
   - The inputs are entered at separate ports – gives high degree of isolation among RF, LO & IF.
   - Converts the RF voltage into a current through trans-conductance.
   - Performs multiplication in current domain.
   - Approximate expression of output current:
     \[ i_{out}(t) = sgn[\cos(w_{LO}t)](IDC + IRF \cos(w_{RF}t)) \]
   - \[ sgn(x) = \frac{4}{\pi} \left[ \sin(x) + \frac{1}{3} \sin^3(x) + \frac{1}{5} \sin^5(x) + \ldots \right] \]
   - The inputs are entered at separate ports – gives high degree of isolation among RF, LO & IF.
   - The inputs are entered at separate ports – gives high degree of isolation among RF, LO & IF.
   - The inputs are entered at separate ports – gives high degree of isolation among RF, LO & IF.
   - The inputs are entered at separate ports – gives high degree of isolation among RF, LO & IF.

**Drawbacks**:
- High LO to IF feed-through, large power consumption compared to previous topology, noise figure.

3. **Double balanced Mixer**
   - Output is balanced to both RF and LO.
   - Has high degree of LO-IF isolation.
   - The LO drive should be large enough, so that the differential pair behaves as switch.
   - Two signals in double balanced mixer are connected in anti-parallel for LO signal but in parallel for RF signal – LO terms sum to zero at output and RF is doubled.
   - Actual current equation can be established on the basis of single stage differential amplifier with time varying large LO in upper part of differential pair and small ac RF signal in lower part of differential pair.
   - Conversion gain:
     \[ \frac{4}{\pi^2} \]

**ADV**:
- Gives higher isolation among RF, LO & IF.
- Gives higher conversion gain.

**DIS ADV**:
- Large power consumption.

Two Important Mixers

**Gilbert Type Mixer**
- Conversion gain = \( g_m R_L \frac{2}{\pi} \)

**Design issues**
- The gain and IIP3 are determined by tail current (I_{ss}). The increase of tail current improves the performance, however the voltage drop across load resistance drives the RF transistor out of saturation. As a result conversion gain and IIP3 suffers.
- Increasing load resistance increases gain, but cannot be increased indefinitely as the RF transistors come out of saturation.

**Even Harmonic Mixer**
- The circuit is a "three level multiplier", composed of two stages, a double-balanced switching cell and a differential transconductance stage.

Low IF Receiver Architecture
Layout of the complete RF Front-End (KGPLPRX)

Freqency Synthesizers

Building blocks of frequency Synthesizer

- PLL based frequency synthesizer is a negative feedback system that locks both phase & frequency.
- Basic building blocks of PLL based frequency synthesizer are:
  - Phase Frequency Detector (PFD) → Sequential tri-state dual DFF PFD
  - Charge Pump → Constant UP/DOWN Current sources with switches on Drain
  - Loop filter → Passive 3rd order low pass filter
  - Voltage Control Oscillator (VCO) → Low KVCO, low KVDD, low phase noise LC VCO with on-chip inductor
  - Programmable Integer N Frequency Divider → Divide by 2/3 peculiar structure with both Current Mode Logic (CML) structure for high frequency division and digital logic structure for low frequency division

Frequency Synthesizer

- Motivation–
  - All frequencies in the band of interest from the reference frequency
  - High degree of purity due to the ever decreasing channel spacing
  - Low power consumption
  - Low cost
  - High integration
  - Explosive growth in demand for wireless communication services
- Direct Analog/Digital Synthesis–
  - Fine frequency resolutions and fast switching times
  - Not suitable for high frequency and low phase noise synthesis
- Indirect PLL based Synthesis–
  - Fine frequency resolutions and fast switching times
  - Suitable for high frequency stability and accuracy, low phase noise and high frequency (even in giga-hertz frequency range) synthesis
  - Amenable to full integration on a standard CMOS technology

Block Diagram of frequency Synthesizer

- Phase → Independent variable.
- For phase variable → VCO is perfect integrator.
- Different blocks modeled as:
  - PFD → Difference Block
  - Charge Pump → Constant gain, (Kcp)
  - Loop Filter → generic Transfer function (F(s))
  - VCO → Integrator with constant gain, (Kvco/s)
  - Frequency Divider → Divider ratio (N)
PLL Large Signal Behavior

- $F_{REF} > F_{VCO/N}$: Equation for Exact PLL locking implies nonlinear phenomena.
- If $F_{VCO/N}$ output of PFD will turn enable more often than Up.
- Loop filter control voltage goes down $\rightarrow$ $F_{VCO}$ goes down.
- Typically, $ts = 25/F_{REF}$: Settling time.

Phase Frequency Detector

- Gives difference between Reference and output phases.
- Usually implemented digitally.
- Most widely used topology $\rightarrow$ Sequential tri-state dual DFF PFD.

Charge Pump

- Gives infinite DC gain with passive filters $\rightarrow$ Needed for zero phase error.
- Consists of two or more Current sources, switched ON/OFF by PFD outputs.
- Mismatches & Leakage in charge pump $\rightarrow$ Spurious component in PLL output.
- Three main topologies:
  - Switch on Source $\rightarrow$ Fastest, Lowest mismatches, Minimum overshoots, easily scalable.

Loop Filter

- Usually a Low pass filter.
- Provides a stabilizing zero for the loop (C2, R2).
- Determines loop’s transient behavior.
- Active or passive implementation possible.
- Passive filter $\rightarrow$ No active device noise, easy on-chip implementation.
- Filter order $\rightarrow$ decides spurious suppression (typically 2-3).

VCO

- VCO parameters, most relevant to Frequency Synthesizers:
  1. $K_{VCO}$ requirements $\rightarrow$ Should be linear
  2. Phase Noise $\rightarrow$ Should meet the specifications
  3. Settling time $\rightarrow$ Should be much higher than PLL loop bandwidth
  4. VCO isolation $\rightarrow$ Buffers should be added at the output
  5. Power consumption $\rightarrow$ Should conform the system requirements.
- Details of VCO design has been discussed in previous chapter.

Programmable Divider

- Only block (except VCO) that operates at RF frequency.
- Implementation is critical $\rightarrow$ Power hungry, high speed.
- Most popular Architecture $\rightarrow$ based on Pre-scalar.
- Only pre-scalar operates at highest frequency.
- Output Frequency $= P*N + A$
- Pre-scalar $\rightarrow$ Current Mode Logic (CML)
- CML $\rightarrow$ Constant current, No power line spikes, Low power at GHz frequencies.
Prescalar architecture → Not modular
→ Complex Layout
Architecture based on 2/3 divider cells:
- Programmable 2/3 divider cells are cascaded.
- For N cells, Division range: 2^N – (2^N+1 – 1).
- Highly regular structure.

Simulation & Silicon Tested Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulation Result</th>
<th>Results Tested on fabricated chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency range of operation</td>
<td>2.4 GHz - 2.4855 GHz</td>
<td>2.3964 GHz - 2.4788 GHz</td>
</tr>
<tr>
<td>No of channels</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Channel spacing</td>
<td>50MHz</td>
<td>50MHz</td>
</tr>
<tr>
<td>VCO gain</td>
<td>60 MHz / V</td>
<td>-</td>
</tr>
<tr>
<td>VCO current</td>
<td>2.5 mA</td>
<td>-</td>
</tr>
<tr>
<td>Charge pump current</td>
<td>50uA</td>
<td>-</td>
</tr>
<tr>
<td>Division ratio</td>
<td>480 - 495</td>
<td>480 - 495</td>
</tr>
<tr>
<td>Open loop unity gain</td>
<td>100 kHz</td>
<td>-</td>
</tr>
<tr>
<td>Phase margin</td>
<td>50 degree</td>
<td>-</td>
</tr>
<tr>
<td>Total power consumption</td>
<td>9 mW</td>
<td>9mW</td>
</tr>
</tbody>
</table>

Layout of Frequency Synthesizer
And Test Setup of the chip

Die area: 1812.4um x 1965.04um
Snapshot of the PCB

Silicon Testing : PLL locking check
(Fref=5MHz).

Divider output when no input is given; Unlocked condition
Divider output when 5MHz input is given; locked condition

Channel selection by Divider control in locked condition

There are 8 control bits used to select a channel among the 16 channels over the frequency range of operation. The divider ratio is changed with change of control bits. Only 4 LSB bits are used to select out of band frequency. The test results are shown in the following table:

<table>
<thead>
<tr>
<th>4 LSB: 4 LSB divider control bits</th>
<th>VCO freq measured GHz</th>
<th>Ideal output as 5MHz reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1110,1000 (480)</td>
<td>2.4926</td>
<td>2.44</td>
</tr>
<tr>
<td>1110,0000 (480)</td>
<td>2.3964</td>
<td>2.44</td>
</tr>
<tr>
<td>1110,1111 (495)</td>
<td>2.4706</td>
<td>2.475</td>
</tr>
<tr>
<td>1110,1100 (492)</td>
<td>2.4686</td>
<td>2.46</td>
</tr>
<tr>
<td>1110,0100 (484)</td>
<td>2.4196</td>
<td>2.44</td>
</tr>
</tbody>
</table>

For first phase of testing, we taken the reference frequency from a signal generator, which gives frequency variation from 4.992M-5.008MHz instead of fixed 5MHz, that’s why the comparison table are slightly mismatched.

Channel selection by Divider control in locked condition

Divider ratios: 1110.0000 (480)
Divider ratios: 1110.0000 (480)

For first phase of testing, we taken the reference frequency from a signal generator, which gives frequency variation from 4.992M-5.008MHz instead of fixed 5MHz, that’s why the comparison table are slightly mismatched.
VCO centre frequency tuning

- There are 5 control bits used to compensate the VCO center frequency variation due to process. These are shown in the following table:

<table>
<thead>
<tr>
<th>Cap. (bit)</th>
<th>VCO freq measured GHz</th>
<th>Divider o/p MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000</td>
<td>2.484</td>
<td>5.536</td>
</tr>
<tr>
<td>00110</td>
<td>2.440</td>
<td>5</td>
</tr>
<tr>
<td>00111</td>
<td>2.414</td>
<td>4.488</td>
</tr>
<tr>
<td>11111</td>
<td>1.970</td>
<td>4.012</td>
</tr>
</tbody>
</table>

**Comparison of performance**

- The frequency synthesizer consumes very low power which is lowest reported till now for integer-N frequency synthesizers in 2.4GHz ZigBee application.
- This structure gives low KNO and KVID.
- The reference signal is generated through a signal generator rather than from a crystal oscillator, thus we expect better phase noise performance of the frequency synthesizer by using crystal.
- Setting time measurement of FRS is on process.

**Supplementary voltage variation and operating current**

<table>
<thead>
<tr>
<th>Conditions</th>
<th>VDD</th>
<th>Supply Current (I(VDD))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum supply voltage for which the chip is functional</td>
<td>1.40V</td>
<td>3.4mA</td>
</tr>
<tr>
<td>Maximum Supply voltage checked</td>
<td>2.5V</td>
<td>8.2mA</td>
</tr>
<tr>
<td>Normal Operating Condition</td>
<td>1.8V</td>
<td>5mA</td>
</tr>
</tbody>
</table>

**References**

• [33] B.S. Carson, High-Frequency Amplifiers, John Wiley & Sons, 1982
• [39] IEEE 802.11b Draft Supplement to-Standard Technology Telecommunications and Information Exchange between Systems Local and Metropolitan Area Networks